module p8(Z, D, S);

output Z;

input[15:0] D;

input[3:0] S;

not n0(inv\_S0, S[0]);

not n1(inv\_S1, S[1]);

not n2(inv\_S2, S[2]);

not n3(inv\_S3, S[3]);

and a0 (a0\_o, D[0], inv\_S1, inv\_S0);

and a1 (a1\_o, D[1], inv\_S1, S[0]);

and a2 (a2\_o, D[2], S[1], inv\_S0);

and a3 (a3\_o, D[3], S[1], S[0]);

or o0 (M0, a0\_o, a1\_o, a2\_o, a3\_o);

and a4 (a4\_o, D[4], inv\_S1, inv\_S0);

and a5 (a5\_o, D[5], inv\_S1, S[0]);

and a6 (a6\_o, D[6], S[1], inv\_S0);

and a7 (a7\_o, D[7], S[1], S[0]);

or o1 (M1, a4\_o, a5\_o, a6\_o, a7\_o);

and a8 (a8\_o, D[8], inv\_S1, inv\_S0);

and a9 (a9\_o, D[9], inv\_S1, S[0]);

and a10 (a10\_o, D[10], S[1], inv\_S0);

and a11 (a11\_o, D[11], S[1], S[0]);

or o2 (M2, a8\_o, a9\_o, a10\_o, a11\_o);

and a12 (a12\_o, D[12], inv\_S1, inv\_S0);

and a13 (a13\_o, D[13], inv\_S1, S[0]);

and a14 (a14\_o, D[14], S[1], inv\_S0);

and a15 (a15\_o, D[15], S[1], S[0]);

or o3 (M3, a12\_o, a13\_o, a14\_o, a15\_o);

and a16 (a16\_o, M0, inv\_S3, inv\_S2);

and a17 (a17\_o, M1, inv\_S3, S[2]);

and a18 (a18\_o, M2, S[2], inv\_S3);

and a19 (a19\_o, M3, S[2], S[3]);

or o4 (Z, a16\_o, a17\_o, a18\_o, a19\_o);

endmodule

module tb\_p8();

reg[15:0] D;

reg[3:0] S;

wire Z;

integer i,j;

p8 UUT(Z,D,S);

initial

begin

#10 $monitor("UUT | D = %b", D, " | S = %b", S, " | Z = ", Z);

for (i=0; i<=15; i=i+1)

begin

D=$urandom%2\*\*16;

for (j=0; j<=15; j=j+1)

begin

S=j;

#10;

end

end

end

endmodule

